Having thus described the invention, what is claimed as new and secured by Letters Patent is:

Claims

1. An apparatus for processing N number of input signals having a common frequency, said apparatus comprising:

at least N-1 number of modulators for modulating N-1 of said N number of input signals into N-1 number of modulated signals;

a combiner for combining said modulated signals along with one non-modulated signal into an aggregate signal;

at least N-1 number of circulators for receiving at least part of said aggregate signal;

N-1 number of demodulators for demodulating said aggregate signal, each said demodulator corresponding to one of said modulators; and

N number of duplexer filters each corresponding to one of said N number of input signals;

wherein said circulators, said demodulators, and said duplexer filters, are arranged so as to pass N number of demodulated portions of said aggregate signal to a corresponding output and each of said demodulated portions being substantially identical to one of said N number of input signals.

2. The apparatus as claimed in Claim 1 wherein said aggregate signal passes serially through said circulators and said demodulators beginning with a first one of said circulators and ending with a last one of said demodulators.

3. The apparatus as claimed in Claim 2 wherein said first one of said circulators is coupled to one of said duplexer filters arranged to pass said one non-modulated signal.

4. The apparatus as claimed in Claim 3 wherein a length of cabling is placed between said combiner and said first one of said circulators.

5. The apparatus as claimed in Claim 4 wherein said length of cabling spans at least a portion of an antenna structure.

6. The apparatus as claimed in Claim 5, further including a plurality of amplifiers each located such that said input signals pass through a respective one of said plurality of amplifiers prior to passing through said at least N-1 number of modulators.

7. The apparatus as claimed in Claim 6 wherein said input signals are forward link transmissions and said plurality of amplifiers are high power amplifiers.

8. The apparatus as claimed in Claim 6 wherein said input signals are reverse link transmissions and said plurality of amplifiers are low power preamplifiers.

9. The apparatus as claimed in Claim 5 wherein said input signals are forward link transmissions and said apparatus further includes a single high power amplifier for amplifying said aggregate signal, said high power amplifier located between said combiner and said length of cabling.

10. The apparatus as claimed in Claims 7, 8, or 9 wherein said modulators and said demodulators operate via a modulation scheme using Walsh codes.

11. The apparatus as claimed in Claims 7, 8, or 9 wherein said modulators and said demodulators operate via a modulation scheme using Serrodynes.

12. A method for processing N number of input signals having a common frequency, said method comprising:

obtaining N number of input signals having a common frequency;
modulating N-1 number of said input signals via a modulation scheme;
combining said input signals after modulation to form an aggregate signal;
transmitting said aggregate signal across a length of cabling; and

demodulating and filtering said aggregate signal through a series of circulators, duplexers, and demodulators such that said aggregate signal is separated into constituent signals each corresponding to each one of said input signals.

13. The method as claimed in Claim 12, further including between said obtaining step and said modulating step, amplifying said input signal via a plurality of amplifiers.

14. The method as claimed in Claim 13 wherein said input signals are forward link transmissions and said plurality of amplifiers are high power amplifiers.

15. The method as claimed in Claim 13 wherein said input signals are reverse link transmissions and said plurality of amplifiers are low power preamplifiers.

16. The method as claimed in Claim 12 wherein said input signals are forward link transmissions and said method further includes between said combining step and said transmitting step, amplifying said aggregate signal via a single high power amplifier.

17. The method as claimed in Claims 14, 15, or 16 wherein said modulation scheme uses Walsh codes.

18. The apparatus as claimed in Claims 14, 15, or 16 wherein said modulation scheme uses Serrodynes.

19. An apparatus for processing N number of modulated, combined, and amplified input signals having a common frequency, said apparatus comprising:

a demodulator for demodulating an amplified aggregate signal consisting of said input signals, said demodulator including

a least N-1 number of circulators for receiving at least part of said aggregate signal;

N-1 number of demodulators for demodulating said aggregate signal; and

N number of duplexer filters each corresponding to one of said N number of input signals;

wherein said circulators, said demodulators, and said duplexer filters are arranged so as to pass N number of demodulated portions of said aggregate signal to a corresponding output, each of said demodulated portions being substantially identical to one of said N number of input signals.